

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Kanji NATORI

Application No.: New U.S. Patent Application

Filed: December 8, 2003

Docket No.: 118008

For: NONVOLATILE SEMICONDUCTOR MEMORY DEVICE
INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

- ☒ 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date of this non-CPA application, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.
- ☒ 2. Relevance of the non-English language references 6, 10 & 11 are discussed in the present specification.
- ☒ 3. The present application was filed or entered the U.S. National Stage of the PCT after June 30, 2003. In accordance with the June 11, 2003, Notice waiving the requirements of 37 C.F.R. §1.98(a)(2)(i), copies of any U.S. patents and patent application publications are not attached.
- ☒ 4. English-language Abstracts of the non-English language references 8-12 are attached hereto.
- ☒ 5. A computer-generated English translation of the following Japanese Patent Publication has been obtained from the website of the Japanese Patent Office ([<http://www.jpo.go.jp>]), and is attached, but has not been reviewed for accuracy. See Reference 8-13.

Respectfully submitted,



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Form PTO-1449 (REV. 8-83)		US Dept. of Commerce PATENT & TRADEMARK OFFICE		ATTY DOCKET NO. 118008		APPLICATION NO. New U.S. Patent Application	
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)				APPLICANT Kanji NATORI			
				FILING DATE December 8, 2003			
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	
	1	US 6,248,633 B1	6/19/2001	OGURA et al.			
	2	US 6,177,318 B1	1/23/2001	OGURA et al.			
	3	5,494,838	2/27/1996	CHANG et al.			
	4	5,422,504	6/6/1995	CHANG et al.			
	5	5,969,383	10/19/1999	CHANG et al.			
	6	5,408,115	4/18/1995	CHANG			
	7	US 6,255,166 B1	7/3/2001	OGURA et al.			
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	
	8	JP A 2001-156188 w/ Abst & Trans	6/8/2001	Japan			
	9	JP A 07-161851 w/ Abst & Trans	6/23/1995	Japan			
	10	JP A 06-181319 w/ Abst & Trans	6/28/1994	Japan			
	11	JP A 11-074389 w/ Abst & Trans	3/16/1999	Japan			
	12	JP A 2002-313090 w/ Abst & Trans	10/25/2002	Japan			
	13	JP B1 2978477 w/ Translation	9/10/1999	Japan			
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)							
	14	Yutaka HAYASHI et al., "Twin MONOS Cell with Dual Control Gates", 2000 Symposium on VLSI Technology Digest of Technical Papers.					
	15	Kuo-Tung CHANG et al., "A New SONOS Memory using Source-Side Injection for Programming", IEEE Electron Device Letters, Vol. 19, No. 7, July 1998, Pgs. 253-255.					
	16	Wei-Ming Chen et al., "A Novel Flash Memory Device with Split Gate Source Side Injection and ONO Charge Storage Stack (SPIN)", 1997 Symposium on VLSI Technology Digest of Technical Papers, Pgs. 63-64.					
EXAMINER		DATE CONSIDERED					
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

Date: December 8, 2003